Notice of Allowability	Application No.	Applicant(s)	
	10/781,112	WU, KOUCHENG	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Papers filed 02/18/2004 and 11/09/2005*.

2. ☒ The allowed claim(s) is/are *1-22*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TH

Tu-Tu Ho Nov. 17, 2005

DETAILED ACTION

1. Applicant's Amendment/Argument filed 11/09/2005 has been reviewed and placed of record in the file.

Response to Arguments

2. Applicant's arguments, see Amendment - After Non-Final Rejection, filed 11/09/2005, with respect to the 103-rejection, mailed 07/12/2005, have been fully considered and are persuasive. The 103-rejection of claims 1-6 and the consequent objection of claims 7-8 have been withdrawn.

Specifically, although Lin in the prior art of record (Lin et al. U.S. Patent 5885868 and 5796142) is silent about a specific structure for the semiconductor electrically-erasable programmable read-only memory (EEPROM) devices, i.e., Lin does not specify whether the device is a NAND-type or a NOR-type device, the structure of Lin's device should be a non-NAND device because a NAND device of the prior art of record, as the prior art of record and the prosecution history indicate, does not comprise both source lines and drain lines as clearly depicted in Fig. 8 of the Lin's references.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR

1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

If an amendment by Applicant is to be filed, Applicant is reminded of the proper format for amendment under Revised Amendment Practice (37 CFR 1.121) as applied to Implement Electronic Maintenance of Official Patent Application Records and as applied to amendments filed after July 30, 2003.

For a sample amendment document and other questions concerning the new practice, please visit the USPTO website at http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/moreinfoamdtprac.htm

4. This application is in condition for allowance except for the presence of claims 23-32 non-elected without traverse. Accordingly, claims 23-32 have been cancelled.

Allowable Subject Matter

5. Claims 1-22 (of "Claims - 02/18/2004") are allowable over the prior art of record.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor device having an electrically erasable programmable read only memory (EEPROM) with all exclusive limitations as recited in claims 1 and 20, comprising a contactless array of EEPROM memory cells disposed in rows and columns and constructed over a silicon-on-insulator (SOI) wafer, each EEPROM memory cell comprising a drain region, a source

region, a gate region, and a body region; a plurality of gate lines each connecting the gate regions of a row of EEPROM memory cells; a plurality of source lines or a plurality of source lines and body lines each connecting the source regions and the body regions of a column of EEPROM memory cells; and a plurality of drain lines each connecting the drain regions of a column of EEPROM memory cells; wherein the source lines and the drain lines are buried lines and the source regions and the drain regions of a column of the EEPROM cells are insulated from the source regions and the drain regions of the adjacent columns of the EEPROM cells; and wherein

the limitations "the source regions and the drain regions" and "insulated" in "the source lines and the drain lines are buried lines and the source regions and the drain regions of a column of the EEPROM cells are insulated from the source regions and the drain regions of the adjacent columns of the EEPROM cells" have been fully considered, namely, the source regions and the drain regions are the source regions and the drain regions as understood from the integral structural views, and not in a wiring diagram view.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

FIG. **8b** is a schematic diagram showing another example of threshold voltage distributions of memory cells in the programmed and erased states in accordance with the present invention.

FIG. **9** is a circuit diagram of the memory array in accordance with the present invention wherein, in each column, the body line is connected to the source line.

FIG. **10a** is a schematic diagram showing one example of threshold voltage distributions of multilevel memory cells in accordance with the present invention.

FIG. **10b** is a schematic diagram showing another example of threshold voltage distributions of multilevel memory cells in accordance with the present invention.

FIG. **11a** is a circuit diagram showing one example of the parallel MLC program operation in accordance with the present invention in which different specified voltages are simultaneously applied to the drain lines.

FIG. **11b** is a circuit diagram showing another example of the parallel MLC program operation in accordance with the present invention, in which different specified voltages are simultaneously applied to the source lines (= body lines).

FIG. **12** is a schematic diagram illustrating the broadened threshold voltage distributions for multilevel memory cells.

FIG. **13** is a flow chart of the bit-by-bit Vt correction operations in accordance with the present invention, in which ProgUp and ProgDn operations are defined in TABLES 2-5.

FIG. **14** is a circuit diagram of a NOR-type contactless flash array on SOI in accordance with one embodiment of the present invention.

FIG. **15** is a circuit diagram of a NOR-type contactless flash array on SOI in accordance with another embodiment of the present invention.

FIG. **16** is a layout plan view of the memory array portion in accordance with an embodiment of the present invention.

FIGS. **17a-i** illustrate sectional views of the memory cell structures at different steps of the manufacturing process of the flash memory device in accordance with the present invention.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
November 17, 2005